REMARKS

In the Office Action, the Examiner noted that claims 1-31 are pending in the application and that claims 1-31 are rejected. By this response, claims 1, 15, 20, and 25 are amended. Claims 19 and 24 are cancelled. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. §103

The Examiner rejects claims 1-31 as being unpatentable over U.S. Publication No. 2003/0172176 by Fidler et al. ("Fidler") in view of U.S. Publication No. 2004/0111537 by Conner et al. ("Connor"). The rejection is respectfully traversed.

More specifically, the Examiner cites FIGs. 1 and 2 of Fidler as showing a DMA controller (18), a MAC (16) coupled to the DMA controller by a streaming interface (FIFO 22), a transmit peripheral configured to receive a communication sequence from the DMA controller, and a receive peripheral configured to transmit a communication sequence to the DMA controller. (Office Action, p. 2). The Examiner equates the DMA controller (18) and the digital controller (32) of Fidler to the transmit and receive peripherals recited in Applicants' claims. The Examiner concedes that Fidler does not specifically teach the exact details of a DCR bridge or logic for handling checksum data, header, footer, data section, control data, or DMA descriptors. (Office Action, p. 3). The Examiner states, however, that such features are common knowledge in the art, as evidenced by Conner.

The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. In particular, Fidler does not teach or suggest a transmit peripheral having a first streaming interface, and a receive peripheral having a second streaming interface. As shown in Fidler, the MAC controller (16) is coupled to the DMA controller (18) using a FIFO (22). To the extent the FIFO is a streaming interface, it is only a single streaming interface between the MAC (16) and the DMA controller (18). Applicants claim two streaming interfaces, one for the transmit peripheral and another for the

receive peripheral. Applicants have clarified that claim 1 includes two streaming interfaces by amending claim 1 to recite first and second streaming interfaces. (See also, Applicants' specification, FIG. 19). Fidler does not teach or suggest two peripherals (one transmit, one receive), each having a separate streaming interface.

Conner generally teaches a computer system that defers operating processing of previously issued operations depending on whether such operations are currently being processed. (Conner, Abstract). Conner does not teach or suggest any peripheral coupled to a streaming interface, in particular, transmit and receive peripherals each having a streaming interface. Since neither Fidler nor Conner teaches or suggests such a feature, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in claim 1. Independent claim 25 recites features similar to those in claim 1 emphasized above. Applicants contend that no combination of Fidler and Conner renders obvious claim 25 for the same reasons discussed above.

Independent claim 20 recites a method of communicating data between a network transceiver and memory circuitry. A communication sequence is transmitted over a streaming interface to a DMA controller. The communication sequence includes a header, a data section, and a footer, where the data section includes data to be written to the memory circuitry. The Examiner cites the data packet (34) in Fidler, shown in FIG. 2 as teaching the claimed communication sequence. Applicants have amended claim 20 to clarify that the communication sequence is transmitted over a streaming interface to the DMA controller. The data packet (34) in Fidler is not transmitted to the DMA controller (18) over a streaming interface. Rather, the data packet (34) is a packet received from the network 12 at the physical layer 14. The MAC controller (16) in Fidler only sends the data field of the packet (34) to the DMA controller, not the entire packet (34). (See Fidler, paragraph 0020). Fidler does not teach or suggest transmitted the claimed communication sequence to the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in claim 20.

Claim 15 recites a method of communicating data between a network transceiver and memory circuitry. A communication sequence is received over a streaming interface from a DMA controller. Similar to claim 20, the communication sequence includes a header, a data section, and a footer. As described above, the packet (34) is transmitted over the network (12) in Fidler, and is not passed to or from the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in claim 15.

Claims 2-14, 16-18, 20-23, and 25-31 depend from claims 1, 15, 20, and 25 and recite additional features thereof. Since the combination of Fidler and Conner does not render obvious Applicants' invention recited in claims 1, 15, 20, and 25, the cited combination does not render obvious Applicants' invention recited in dependent claims 2-14, 16-18, 20-23, and 25-31.

In view of the foregoing, Applicants contend that claims 1-18, 20-23, and 25-31 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103. Claims 19 and 24 have been cancelled and thus the rejection of such claims is moot. Applicants respectfully request that the present rejection be withdrawn.

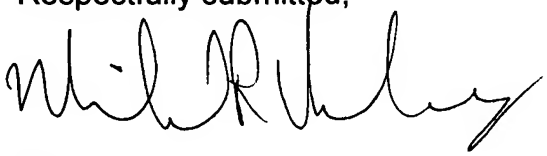
CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Michael Hardaway at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



Michael R. Hardaway
Attorney for Applicants
Reg. No. 52,992

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 1, 2007.

Julie Matthews
Name

Signature